REMARKS

Preliminarily, Applicants respectfully request the Examiner to complete the first page of the Office Action Summary to show that all of the certified copies of the priority documents have been received.

Claims 1, 2 and 4 have been amended to recite that the printed wiring substrate has a planar surface, and that the plurality of capacitor terminals projects beyond the planar surface of the printed wiring substrate. Support is found, for example, by reference to Fig. 1, showing planar surface 120A and capacitor terminals 131 projecting beyond planar surface 120A.

Support for new claims 16-18 is found, for example, at page 42, lines 2-3 (core substrate made of resin); at page 15, lines 10-12 (capacitor accommodation cavity); and at page 44, lines 5-13 (capacitor comprising a dielectric layer made of ceramic and electrodes arranged in alternating layers).

Entry of the amendments is respectfully requested.

Review and reconsideration on the merits are requested.

Claims 1-15 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,218,729 to Zavrel, Jr. et al. The Examiner considered Zavrel as meeting each of the terms of the rejected claims, including a printed wiring substrate 822 having a built-in capacitor 804 on which an IC chip 820 is mounted. In reference to Fig. 8, the capacitor includes a pair of plate electrodes 860 and 862 and vias 850 and 854 extending to substrate terminals 840 and 842. The Examiner considered vias 850 and 854 to be within the scope of the claimed capacitor terminals connected to the electrodes (plates) of the capacitor. IC chip 820 is flip-chip-bonded to pads 840

and 842 via solder bump 828, and also to substrate terminal 856 via pad 844 and solder bump 828.

Applicants respectfully traverse for the following reasons.

The invention differs from Zavrel in that in Zavrel, the embedded capacitor 804 is electrically connected to IC chip 820 through vias 850 and 854, pads 840 and 842 and solder bumps 828, whereas in the invention, the capacitor terminals are directly flip-chip-bonded to the IC chip. Therefore, to more clearly define over the applied prior art, claims 1, 2 and 4 have been amended to recite that the printed wiring substrate has a planar surface, and that the plurality of capacitor terminals project beyond the planar surface of the printed wiring substrate. This arrangement, which facilitates connection of the IC chip to the capacitor and printed wiring substrate, is not disclosed by Zavrel.

Another distinction is that although capacitor 804 in Zavrel is a built-in capacitor, it is an embedded capacitor and the printed wiring substrate does not have a capacitor accommodation cavity for accommodating the capacitors claimed, for example, in claim 7 and in new claims 16-18. Rather, the capacitor is formed from opposing metal layers and intervening dielectric constituting part of the substrate itself. There is no capacitor accommodation cavity for accommodating a capacitor separate from the substrate itself.

New claims 16-18 further recite that the capacitor comprises a dielectric layer made of ceramic and alternating electrode layers. This particular arrangement, in combination with the capacitor accommodation cavity, allows the ceramic capacitor 130 to be disposed within the resin substrate 100 as close as possible to the IC chip 101. This particular advantage of the

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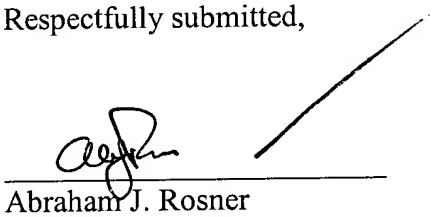
invention, defined in terms of the structure of the claimed printed wiring circuit, is also not disclosed by Zavrel.

For the above reasons, it is submitted that the amended claims are not anticipated by Zavrel, and withdrawal of the foregoing rejection under 35 U.S.C. § 102(e) is respectfully requested.

Withdrawal of all rejections and allowance of claims 1-13 and 16-18 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 14 and 15 are canceled.

The following claims are amended:

1. (Amended) A printed wiring substrate having a planar surface and a built-in capacitor on which an IC chip is mounted, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively flip-chip-bonded to a plurality of connection-to-capacitor terminals of the IC chip; and

the plurality of substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip.

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2. (Amended) A printed wiring substrate having a planar surface and a built-in capacitor on which an IC-chip-carrying printed wiring substrate is mounted, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip-carrying printed wiring circuit comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC-chip-carrying printed wiring substrate; and

the plurality of substrate terminals of the printed wiring substrate are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC-chip-carrying printed wiring substrate.

4. (Amended) A printed wiring substrate having a planar surface and a built-in capacitor for mounting an IC chip or IC-chip-carrying printed wiring substrate having a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals, characterized in that:

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the capacitor comprises:

a pair of electrodes or electrode groups; and

a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC chip or IC-chip-carrying printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups; and

the printed wiring substrate comprises a plurality of substrate terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC chip or IC-chip-carrying printed wiring substrate.

Claims 16-18 are added as new claims.